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A Noise Tolerant and Low Power Dynamic Logic Circuit Using Finfet Technology

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Abstract: For the improvement of performance and noise tolerance in dynamic logic circuits, a technique is proposed in this paper. A two-input AND gate is designed and simulated in 32nm technology using FinFET device. Simulation results indicate that the proposed technique provides improvement in noise tolerance of about three times and the use of FinFET device reduces the power consumption over the conventional MOSFET designs.
Keywords: FinFET, Noise Tolerance, ANTE, Power Consumption, MOSFET

I.   Introduction

The scaling of conventional MOS transistor has become increasingly difficult because of its large short channel effects. Aggressive scaling of MOS device dimensions also leads to lower noise tolerance and higher average power consumption.

Fin-type field effect transistors (FinFET) are promising substitute for bulk MOS at the nanoscale. This is because the fabrication technology of FinFET is almost the same as that of the conventional MOS transistor [1]. FinFET's are from the double gate transistors family and are quasi-planar in nature. They are termed as quasi-planar because the current direction is parallel to its wafer and the channel is formed perpendicular to it.

FinFET's gate terminal can either be shorted or independently controlled to offer rich design space [3]. The two electrically coupled gates and thin silicon body of the FinFET are known to suppress the short channel effects.

Dynamic MOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. Noise is a major issue in design of dynamic logic circuits. In deep submicron region noise tolerance of dynamic logic circuit is very poor and they are more prone to logic failure [4]. There are various noise sources in dynamic logic circuits which are charge sharing noise, leakage noise, crosstalk noise, power and ground noise, substrate noise, etc. FinFET's having diverse design options and better control over channel provides low power configurations and higher noise tolerance.

In this paper, we propose a technique that is noise tolerant and has low power dynamic logic circuit and is designed using FinFET technology. We have designed a two-input AND gate dynamic logic circuit which is simulated on HSPICE in 32nm technology. This paper is organized as follows: Section 1 gives brief introduction to the research work. Section 2 briefs about FinFET technology, includes literature survey and latest developments on FinFET technology. Section 3 and 4, describe two of the existing dynamic logic techniques in MOSFET that are implemented using FinFET technology. Proposed noise tolerant technique is described in Section 5. In Section 6, methodology and metrics used for analysis are presented and in Section 7 and 8 simulations results and conclusion are presented.

II.   FinFET Technology

A double gate transistor is built on an SOI substrate, and is based on the earlier DELTA (single gate) transistor design. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device [5]. Over 32nm technology, there is significant reduction in power consumption when FinFET is used instead of MOSFET. The basic structure of FinFET is shown in Figure 1.
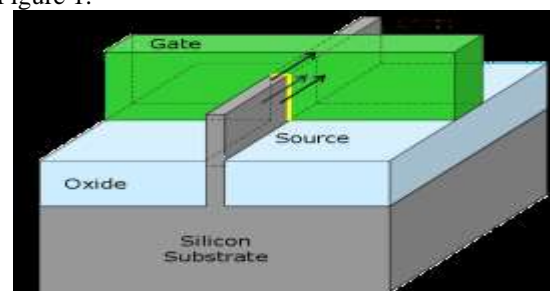

Figure 1: Structure of FinFET[5]

The FinFET device structure consists of a silicon fin surrounded by shorted or independent gate on either side of the fin, typically on silicon insulator substrate.

FinFET has two gates, which can be operated independently or tied together. The threshold voltage at one gate can be controlled with the help of voltage at the other gate. Figure 2, shows the FinFET in different configurations and Figure 3 shows the I_D-V_{DS} characteristics with varying V_{GS} in n-type FinFET device [9].

In the single-gate mode, the short channel effects (threshold voltage roll- off, sub threshold swing degradation and drain induced barrier lowering) are actually less severe than those of the device in the double-gate mode [2].
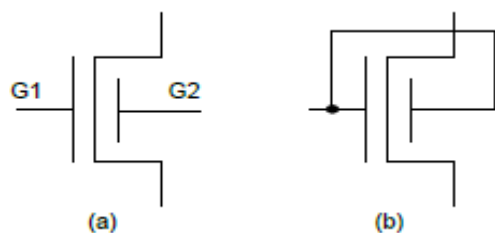

Figure 2: FinFET Configurations (a) Independent Gates (b) Shorted Gates [9]

FinFET devices can be used to increase the performance by reducing the leakage current and power dissipation, because front and back gates both can be controlled independently or both simultaneously [11].
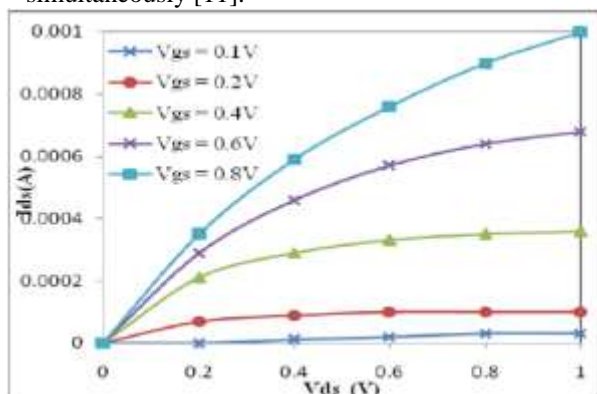

Figure 3: I_D-V_{DS} double-gate n-type FinFET Device of gate length L = 32 nm [9]

The effective width of a FinFET device is quantized due to the vertical gate structure. The fin height determines the minimum width with the two gates tied together, W_{min} is given by,

$$W_{min} = 2.H_{fin} + t_{si}$$

Where, Hfin is fin height and tsi is the thickness of silicon body [6]. Typically, the fin thickness is kept smaller than the fin height to reduce the short channel effects. The FinFET height H_{fin}, together with the fin pitch (determined by photolithography) defines the

FinFET device width Wfin within the given silicon width of the planar device, to get the same or better device strength [8].

The key benefits of FinFET technology over MOSFET includes low off currents, higher on currents, lower average power consumption and reduces short channel effects (SCEs) [10].

Research groups and companies such as Intel, IBM, have shown interest in developing similar devices, as well as mechanisms to migrate mask layouts from bulk MOSFET to FinFET [10].

III. Domino Logic Technique using FinFET:

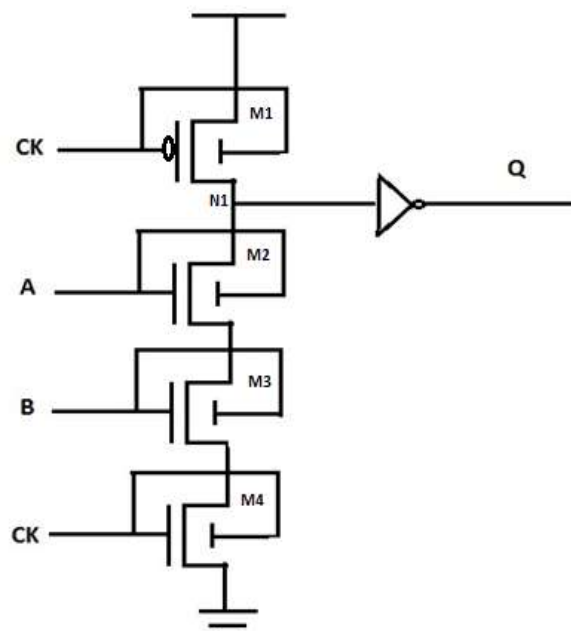Figure 4, shows the schematic of a two input domino AND gate using FinFET technology.

Figure 4: Domino Logic Technique using FinFET

The Domino logic circuit works under two phases, namely, precharge phase and evaluation phase. When CK = 0 (Precharge Phase) the internal node (N1) is precharged to Vdd as M1 is on and M4 is off (disabled pull down) which means that there is no path to ground. When CK =1 (Evaluation Phase), M1 is off and M4 is on. According to the inputs, the output is evaluated. The two gates are tied together in the schematic to form short gate configuration of the FinFET. The inverter at the output gives the standard Domino Logic functionality. In Domino Logic, inputs must be stable before CK goes high because once output has been discharged it will not go high again until the next cycle of CK.

IV. Twin Transistor Technique using FinFET:

For the improvement in the noise tolerance of the dynamic logic circuits, a number of techniques have been previously introduced using MOSFET like Twin Transistor Technique, Mirror and Triple Transistor Technique. We have implemented the Twin Transistor Technique using FinFET device in short gate configuration.

Figure 5, shows the twin transistor technique schematic using FinFET technology.
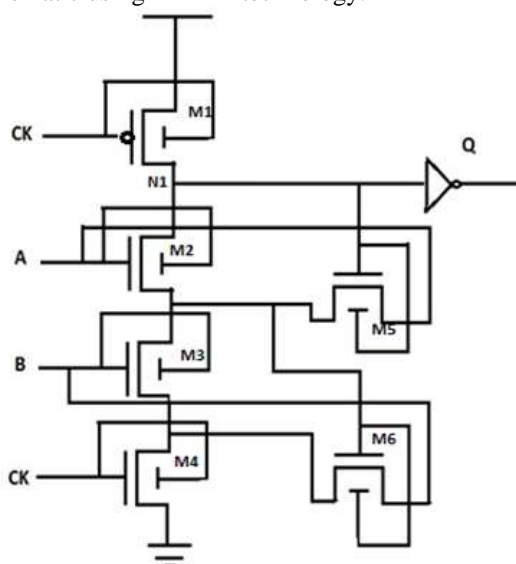

Figure 5: Twin Transistor Technique using Short Gate FinFET

In this technique, two transistors M5 and M6, named as twin transistors are added in the Domino Logic circuit. The purpose of adding twin transistors is to increase the turn on voltage (threshold voltage) of the Pull Down network (PDN). This is done by pulling up the voltage of source node of transistor M2 and M3 as shown in Figure 5.

V. Proposed Technique

Figure 6 shows the schematic diagram of our proposed technique for much better noise tolerance using FinFET. The proposed technique has additional transistors added to increase the noise tolerance of the AND Gate. The additional transistors are M2, M5 and M6. The functions of these transistors are explained as follows:
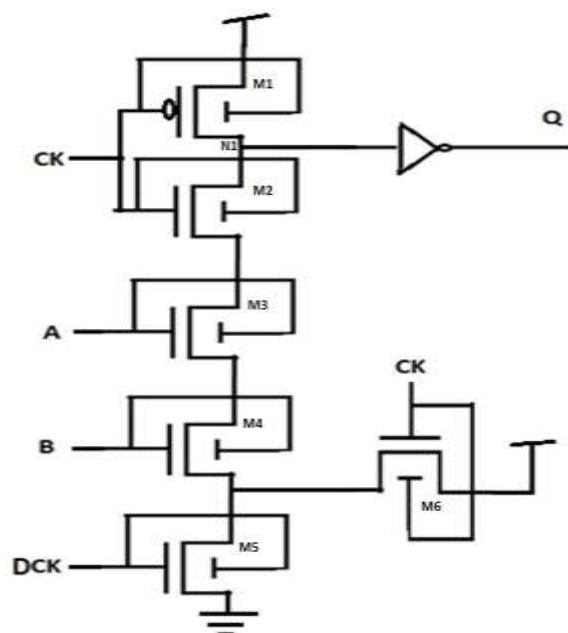

Figure 6: Proposed Technique FinFET

There are two clock signals CK and DCK (Delayed Clock) in this technique. Delayed Clock is generated by delaying the CK signal using a delay circuit. A simple delay circuit consists of a series of inverters. This Delayed Clock signal is fed to M5 transistor which helps in increasing the noise tolerance of the AND gate.

5.1 Improved Noise Tolerance Process of Proposed Technique:

The noise tolerance of the proposed technique is improved by:

M2 as Stacking Transistor: When CK = 0, M1 is on and M2 is off and the node N1 is precharged to Vdd. As transistor M2 is off, there is no leakage path to ground. This reduces the leakage noise in the proposed technique. Charge sharing noise is also reduced as the path to PDN remains closed. This stacking effect improves the noise tolerance.

Raising source voltage of PDN: The threshold voltage of the PDN is improved by raising the source voltage of the PDN. As shown in Figure 6, the transistor M6 is added to increase the common source voltage of the pull down network (PDN). This causes the source body biasing voltage to increase, resulting in the increase of the threshold voltage of the n-type FinFET's in PDN. Thus, the PDN can now tolerate more amount of noise at its inputs.

Delayed Clock (DCK): In the proposed technique, transistor M5 is fed with Delayed clock signal. When CK=1 (Evaluation Phase), M1 is off, M3 is on. The

output is evaluated according to the inputs. As DCK is still low, the transistor M6 is off. This shuts down the path between node N1 and ground. Leakage noise is reduced further and the noise immunity is improved in the proposed technique.

VI.   Methodology

The Domino Logic Technique FinFET, Twin Transistor technique FinFET and the proposed technique is simulated on HSPICE Software tool. The model used for FinFET circuit analysis is BSIM-CMG for 32nm FinFET device.

BSIM-CMG is a model for MG transistors which is implemented in Verilog-A. This model describes all the important behavior of MG transistor. It is physics based model which is scalable and predictive over a wide range of device parameters [12].

A Noise Injection Circuit (NIC) is used to apply noise pulses to one of the inputs of AND gate and other input is set to high logic for noise tolerance measurement. The NIC schematic [7] is shown in Figure 7.
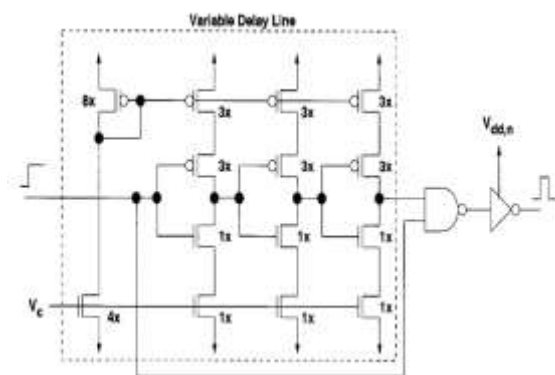

Figure 7: Noise Injection Circuit[7]

This NIC is implemented using FinFET transistors and simulated on HSPICE to give an output of certain amplitude and duration. The output pulse is the noise injected to the AND gate.

To quantify the noise immunity and performance of the techniques, certain metrics are considered. The parameters used for comparison are Average Power Consumption, Average Noise Threshold Energy (ANTE) and Delay. The proposed technique is compared with Domino FinFET and Twin transistor FinFET techniques. A comparative study of proposed technique using FINFET and MOSFET is also analyzed on the basis of average power consumption.

The Average Noise Threshold Energy (ANTE) metric is defined as the average input noise energy that the circuit can tolerate. It is defined mathematically as

$$ANTE = E\ (V_n^2.T_n)$$

Where, V_n is the Amplitude and T_n is the width of the input noise pulse and E( ) is their average [3].

1. Simulation Results

The chart in Figure 8 shows that the Average Noise Threshold Energy (ANTE) of the proposed technique is best amongst all the techniques. The ANTE of proposed technique is about 3.5 times better than that of Domino technique and 2.3 times better than Twin Transistor technique FinFET.
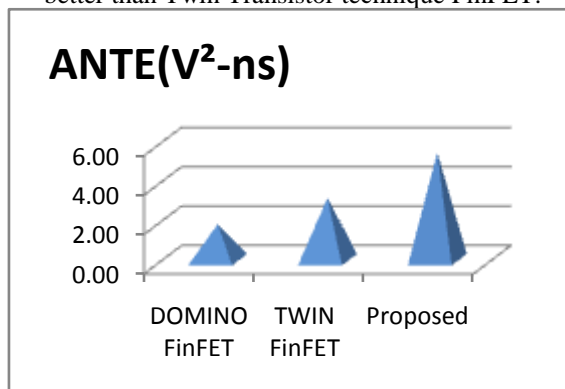

Figure 8: Comparision on the basis of ANTE

The chart shown in Figure 9 shows the average power consumption in the techniques including the Noise Injection Circuit. It indicates that the average power consumption is least in Domino technique. In Twin Transistor technique and proposed technique the Average power is almost same.
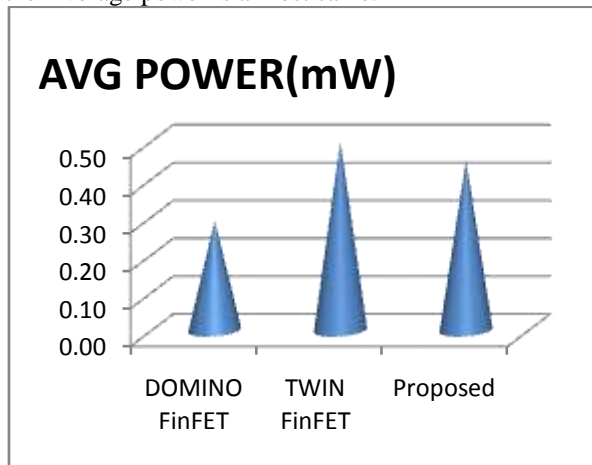

Figure 9: Comparision on the basis of Average Power Consumption

Figure 10, shows bar chart for Delay in the techniques. As the path of signals is same, the delay in Domino technique and Twin Transistor technique is almost same. There is an increase in delay in the proposed technique because of used Delayed Clock signal, which can be adjusted by reducing the delay between the two clock signals.
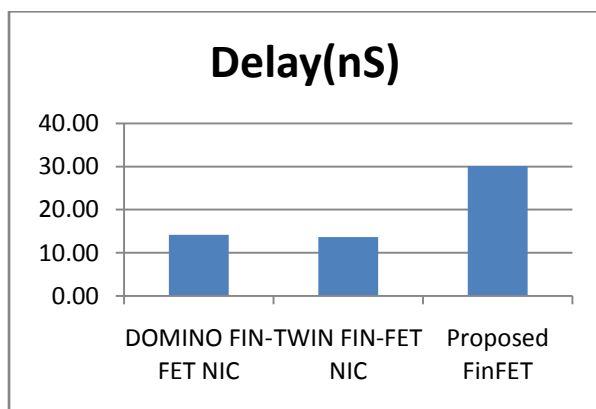
Delay(nS)

Figure 10: Comparision on the basis of Delay

In Figure 11, a pie chart is presented, which clearly states that by the use FinFET over conventional MOSFET a large amount of average power is reduced.
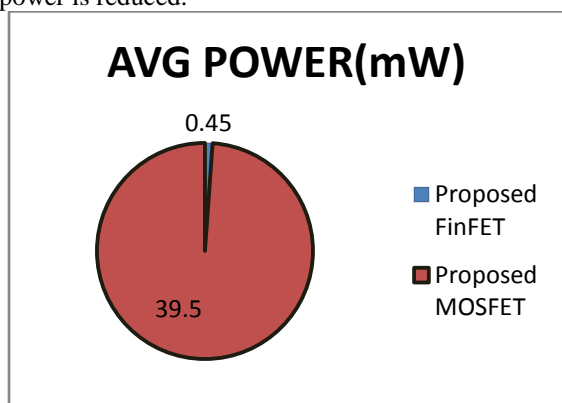
AVG POWER(mW)

Figure 11: Comparison on Average Power between Proposed technique in FinFET and in MOSFET

Table 1 gives details of the Simulation Results of the techniques.

METRIC/ TECHNIQUE	DOMINO FinFET	TWIN FinFET	Proposed FinFET
AVG POWER (mW)	0.29	0.50	0.45
ANTE (V²-ns)	1.81	3.14	5.44
Delay (nS)	14.20	13.66	30.1

Table 1: Performance Comparison For 2-Input AND Dynamic Logic Gate

VII. Conclusion

The use of FinFET over MOSFET in the proposed technique reduces average power consumption. It indicates that FinFET is a promising substitute for MOSFET beyond 32nm technology. The reduced short channel effects in FinFET and better control over the gate of the FinFET improves the average power in designed techniques. As already shown in simulation results, the proposed technique has the highest noise immunity, but this is achieved at the cost of higher delay in the proposed technique.

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